APPENDIX I

ALL PENDING CLAIMS WITH AMENDMENTS EFFECTED THEREIN

1. (Cancel)

2. (Currently Amended) A zero value-detecting circuit, comprising:

an addition means for receiving a 1-bit digital signal produced by encoding an analog signal by delta sigma modulation and taking a sum of said 1-bit digital signals of a given number of samples applied immediately before;

a first decision means for making a decision as to whether said analog signal has a zero value based on the output value from said addition means and for producing a first output signal; and

a second decision means for producing a second output signal indicating that said analog signal assumes a zero value when said first decision means keeps delivering said first signal for a given period of time,

wherein said given number of samples corresponds to N times a number of bits of a repeating pattern appearing in said 1-bit digital signal and corresponding to said delta sigma modulation when said analog signal assumes a zero value, where N is an integer greater than 1.

3. (Currently Amended) A zero value-detecting circuit, comprising:

an addition means for receiving a 1-bit digital signal produced by encoding an analog signal by delta sigma modulation and taking a sum of said 1-bit digital signals of a given number of samples applied immediately before;

a first decision means for making a decision as to whether said analog signal has a zero value based on the output value from said addition means and for producing a first output signal; and

a second decision means for producing a second output signal indicating that said analog signal assumes a zero value when said first decision means keeps delivering said first signal for a given period of time, wherein:

said given number of samples corresponds to N times the number of bits of a repeating pattern appearing in said 1-bit digital signal and corresponding to said delta sigma modulation when said analog signal assumes a zero value,where N is an integer equal to or greater than 1; and

said addition means comprises a shift register having stages corresponding in number to said given number of samples for which said 1-bit digital signal is received and an adder for summing up values at each stage of said shift register, and wherein said first

decision means produces said first signal when a sum value obtained by said adder corresponds to half of said given number of samples.

4. (Currently Amended) A zero value-detecting circuit, comprising:

an addition means for receiving a 1-bit digital signal produced by encoding an analog signal by delta sigma modulation and taking the sum of said 1-bit digital signals of a given number of samples applied immediately before;

a first decision means for making a decision as to whether said analog signal has a zero value based on the output value from said addition means and for producing a first output signal; and

a second decision means for producing a second output signal indicating that said analog signal assumes a zero value when said first decision means keeps delivering said first signal for a given period of time, wherein:

said given number of samples corresponds to N times the number of bits of a repeating pattern appearing in said 1-bit digital signal and corresponding to said delta sigma modulation when said analog signal assumes a zero value, where N is an integer equal to or greater than 1; and

said addition means comprises a shift register having stages corresponding in number to said number of samples for which said

1-bit digital signal is received, a comparison means for comparing the value of the 1-bit digital signal entered into said shift register and the value at the final stage of said shift register and producing a clock signal if they are different, and a counting means of a bit number more than half of said given number of samples, said counting means counting UP in response to said clock signal when the 1-bit digital signal entered into said shift register is at a first logical level and counting DOWN when the 1-bit digital signal applied into said shift register is at a second level, and wherein said first decision means produces said first signal when a count value obtained by said counter corresponds to half of said given number of samples.

5. (New) The zero value detecting circuit of claim 2 wherein said number of bits of the repeating pattern is 8.

6. (New) The zero value detecting circuit of claim 5 wherein said first decision means determines the analog signal has a zero value when the sum is equal to half said given number of samples.

7. (New) The zero value detecting circuit of claim 3 wherein said number of bits of the repeating pattern is 8.

8. (New) The zero value detecting circuit of claim 4 wherein said number of bits of the repeating pattern is 8.